Claims

Having thus described our invention, what we claim as new and desire to secure by Letters Patent is:

1. A layered structure for forming p-channel field effect transistors comprising:

a single crystalline substrate,

a first layer of relaxed $Si_{1-x}Ge_x$ formed epitaxially on said substrate where Ge fraction x is in the range from 0.35 to 0.5,

a second layer of $Si_{1-x}Ge_x$ formed epitaxially on said first layer,

a third layer of undoped Si formed epitaxially on said second layer,

a fourth layer of undoped $Si_{1-x}Ge_x$ formed epitaxially on said third layer,

a fifth layer of Ge formed epitaxially on said fourth layer whereby said fifth layer is under compressive strain and has a thickness less than its critical thickness with respect to said first layer,

a sixth layer of $Si_{1-w}Ge_w$ formed epitaxially on said fifth layer where the Ge fraction w is in the range from 0.5 to <1.0 and where $w\text{-}x > 0.2$ whereby said sixth layer is under compressive strain, and

a seventh layer of $Si_{1-x}Ge_x$ formed epitaxially on said sixth layer.

2. The layered structure of claim 1 further including an over-shoot layer, $Si_{1-y}Ge_y$, within the strain relief structure of said first layer having a Ge fraction y, where $y = x + z$ and z is in the

range from 0.01 to 0.1, and having a thickness less than its critical thickness with respect to said first layer.

3. The layered structure of claim 1 wherein an active device region is a buried composite channel structure made up of an epitaxial Ge channel of said fifth layer and an epitaxial $Si_{1-w}Ge_w$ channel of said sixth layer having a higher compressive strain to provide a deeper quantum well or a higher barrier for better hole confinement as compared to a single layer channel device alone.

4. The layered structure of claim 1 wherein said fifth layer is formed at temperatures where 3D growth of Ge films does not occur to generate interface roughness problems and at a temperature range from 275° - 350° C where 2D growth of Ge films does occur.

5. The layered structure of claim 1 wherein the Ge content *w* may be graded within said sixth layer starting with a higher Ge content nearer said fifth layer and grading down in Ge content towards the upper surface of said sixth layer.

6. The layered structure of claim 1 wherein a spacer region comprises said third layer of strained Si and said fourth layer of relaxed $Si_{1-x}Ge_x$.

7. The layered structure of claim **1** wherein said third layer is under tensile strain and is commensurate having a thickness below its critical thickness with respect to said first layer at its interface with said second layer.

8. The layered structure of claim **1** wherein said second layer is a p-doped $Si_{1-x}Ge_x$ layer formed below a channel region of said fifth and sixth layers and separated therefrom by said third layer of Si and said fourth layer of $Si_{1-x}Ge_x$, said second layer is to having a thickness in the range from 1 to 20 nm with a preferred thickness from 4 to 5 nm and having an electrically active donor dose in the range from 1 to $3x10^{12}$ cm^{-2}.

9. A layered structure for forming p-channel field effect transistors comprising:

a single crystalline substrate,

a first layer of relaxed $Si_{1-x}Ge_x$ formed epitaxially on said substrate where Ge fraction x is in the range from 0.35 to 0.5,

a second layer of $Si_{1-x}Ge_x$ formed epitaxially on said first layer,

a third layer of undoped Si formed epitaxially on said second layer,

a fourth layer of Ge formed epitaxially on said third layer whereby said fourth layer is under compressive strain and having a thickness less than its critical thickness with respect to said first layer,

a fifth layer of $Si_{1w}Ge_w$ formed epitaxially on said fourth layer wherein the Ge fraction w is in the range from 0.5 to <1.0 and where w-x > 0.2 whereby said fifth layer is under compressive strain, and

a sixth layer of $Si_{1-x}Ge_x$ formed epitaxially on said fifth layer.

10. The layered structure of claim **9** further including an over-shoot layer, $Si_{1-y}Ge_y$, within the strain relief structure of said first layer having a Ge fraction y, where $y = x + z$ and z is in the range from 0.01 to 0.1, and having a thickness less than its critical thickness with respect to said first layer.

11. The layered structure of claim **9** wherein an active device region is a buried composite channel structure made up of an epitaxial Ge channel of said fourth layer and an epitaxial $Si_{1-w}Ge_w$ channel of said fifth layer having a higher compressive strain to provide a deeper quantum well or a higher barrier for better hole confinement as compared to a single layer channel device alone.

12. The layered structure of claim **9** wherein said fourth layer is formed at temperatures where 3D growth of Ge films does not occur to generate interface roughness problems and at a temperature range from 275° - 350° C where 2D growth of Ge films does occur.

13. The layered structure of claim **9** wherein the Ge content w may be graded within said fifth layer starting with a higher Ge content nearer said fourth layer and grading down in Ge content towards the upper surface of said fifth layer.

14. The layered structure of claim 9 wherein a spacer region is a single layer structure comprised of said third layer wherein said third layer is strained Si.

15. The layered structure of claim 9 wherein said third layer is under tensile strain and is commensurate having a thickness below its critical thickness with respect to said first layer at its interface with said second layer.

16. The layered structure of claim 9 wherein said third layer Si may be substituted with a relaxed $Si_{1-x}Ge_x$ layer with an adjustable thickness to allow the spacer thickness to be varied accordingly whereby the supply dose may be optimized for device applications as a function of temperature in the range from 0.4 to 425K.

17. The layered structure of claim 9 wherein said second layer is a p-doped $Si_{1-x}Ge_x$ layer formed below a channel region of said fourth and fifth layers and separated therefrom by said third layer of Si.

18. The layered structure of claim 16 wherein the supply layer of said second layer is formed and separated below the channel region of said fourth and fifth layers by said relaxed $Si_{1-x}Ge_x$ layer.

19. A layered structure for forming p-channel field effect transistors comprising:

a single crystalline substrate,

a first layer of relaxed $Si_{1-x}Ge_x$ formed epitaxially on said substrate where Ge fraction x is the range from 0.35 to 0.5,

a second layer of Ge formed epitaxially on said first layer whereby said second layer is under compressive strain and having a thickness less than its critical thickness with respect to said first layer,

a third layer of $Si_{1-w}Ge_w$ formed epitaxially on said second layer where the Ge fraction w is in the range from 0.5 to <1.0 and where $w-x > 0.2$ whereby said third layer is under compressive strain,

a fourth layer of undoped $Si_{1-x}Ge_x$ formed epitaxially on said third layer,

a fifth layer of undoped Si formed epitaxially on said fourth layer, and

a sixth layer of p-doped $Si_{1-x}Ge_x$ formed epitaxially on said fifth layer.

20. The layered structure of claim **19** further including an over-shoot layer, $Si_{1-y}Ge_y$, within the strain relief structure of said first layer having a Ge fraction y, where $y = x + z$ and z is in the range from 0.01 to 0.1, and having a thickness less than its critical thickness with respect to said first layer.

21. The layered structure of claim **19** wherein an active device region is a buried composite channel structure made up of an epitaxial Ge channel of said second layer and an epitaxial $Si_{1-w}Ge_w$ channel of said third layer having a higher compressive strain to provide a deeper quantum well or a higher barrier for better hole confinement as compared to a single layer channel device alone.

22. The layered structure of claim **19** wherein said second layer is formed at temperatures where 3D growth of Ge films does not occur to generate interface roughness problems and at a temperature range from 275° - 350° C where 2D growth of Ge films does occur.

23. The layered structure of claim **19** wherein the Ge content *w* may be graded within said third layer starting with a higher content nearer said second layer and grading down in Ge content towards the upper surface of said third layer.

24. The layered structure of claim **19** wherein a spacer region is a composite layer structure comprising said fifth layer of strained Si and said fourth layer of relaxed $Si_{1-x}Ge_x$.

25. The layered structure of claim **19** wherein said fifth layer is under tensile strain and is commensurate having a thickness below its critical thickness with respect to said first layer at its interface with said second layer.

26. The layered structure of claim 19 wherein the supply layer is a p-doped $Si_{1-x}Ge_x$ layer of said sixth layer formed above a channel region of said second and third layers and is separated by a composite spacer structure of said fifth layer of Si and said fourth layer of $Si_{1-x}Ge_x$.

27. A layered structure for forming p-channel field effect transistors comprising:

a single crystalline substrate,

a first layer of relaxed $Si_{1-x}Ge_x$ formed epitaxially on said substrate where Ge fraction x is the range from 0.35 to 0.5,

a second layer of Ge formed epitaxially on said first layer whereby said second layer is under compressive strain and has a thickness less than its critical thickness with respect to said first layer,

a third layer of $Si_{1-w}Ge_w$ formed epitaxially on said second layer where the Ge fraction w is in the range from 0.5 to <1.0 and where $w-x > 0.2$ whereby said third layer is under compressive strain,

a fourth layer of undoped $Si_{1-x}Ge_x$ formed epitaxially on said third layer, and

a fifth layer of p-doped $Si_{1-x}Ge_x$ formed epitaxially on said fourth layer.

28. The layered structure of claim **27** further including an over-shoot layer, $Si_{1-y}Ge_y$, within the strain relief structure of said first layer having a Ge fraction y, where $y = x + z$ and z is in the range from 0.01 to 0.1, and having a thickness less than its critical thickness with respect to said first layer.

29. The layered structure of claim **27** wherein an active device region is a buried composite channel structure made up of an epitaxial Ge channel of said second layer and an epitaxial $Si_{1-w}Ge_w$ channel of said third layer having a higher compressive strain to provide a deeper quantum well or a higher barrier for better hole confinement as compared to a single layer channel device alone.

30. The layered structure of claim **27** wherein said second layer is formed at temperatures where 3D growth of Ge films does not occur to generate interface roughness problems and at a temperature range from 275° - 350° C where 2D growth of Ge films does occur.

31. The layered structure of claim **27** wherein the Ge content *w* may be graded within said third layer starting with a higher content nearer said second layer and grading down in Ge content towards the upper surface of said third layer.

32. The layered structure of claim **27** wherein a spacer region is a single layer structure comprised of a relaxed $Si_{1-x}Ge_x$ layer of said fourth layer.

33. The layered structure of claim **27** wherein said fourth layer of $Si_{1-x}Ge_x$ may be substituted with a thin strained commensurate Si layer whereby a thin spacer thickness may be provided for a MODFET device.

34. The layered structure of claim **27** wherein said fifth layer is a p-doped $Si_{1-x}Ge_x$ layer formed above a channel region of said second and third layers and separated therefrom by said fourth layer of $Si_{1-x}Ge_x$.

35. The layered structure of claim **33** wherein said fifth layer is a p-doped $Si_{1-x}Ge_x$ layer formed above a channel region of said second and third layers and separated therefrom by a thin strained commensurate Si layer.

36. A field-effect transistor structure consisting of the layered structure of claim 1, further comprising,

electrical isolation regions created by the selective removal of at least said seventh through second layer,

a Schottky gate electrode formed on said seventh layer,

a source electrode located on one side of said gate electrode, and

a drain electrode located on the other side of said gate electrode.

37. A field-effect transistor structure consisting of the layered structure of claim 9, further comprising,

electrical isolation regions created by the selective removal of at least said sixth through second layer,

a Schottky gate electrode formed on said sixth layer,

a source electrode located on one side of said gate electrode, and

a drain electrode located on the other side of said gate electrode.

38. A field-effect transistor structure consisting of the layered structure of claim 1, further comprising,

electrical isolation regions created by the selective removal of at least said seventh through second layer,

a gate dielectric formed on said seventh layer,

a gate electrode on said gate dielectric,

a source electrode located on one side of said gate electrode, and

a drain electrode located on the other side of said gate electrode.

39. A field-effect transistor structure consisting of the layered structure of claim 9, further comprising,

electrical isolation regions created by the selective removal of at least said sixth through second layer,

a gate dielectric formed on said sixth layer,

a gate electrode on said gate dielectric,

a source electrode located on one side of said gate electrode, and

a drain electrode located on the other side of said gate electrode.

40. A field-effect transistor structure consisting of the layered structure of claim 19, further comprising,

electrical isolation regions created by the selective removal of at least said sixth through second layer,

a gate dielectric formed on said sixth layer,

a gate electrode on said gate dielectric,

a source electrode located on one side of said gate electrode, and

a drain electrode located on the other side of said gate electrode.

41. A field-effect transistor structure consisting of the layered structure of claim 27, further comprising,

electrical isolation regions created by the selective removal of at least said fifth through second layer,

a gate dielectric formed on said fifth layer,

a gate electrode on said gate dielectric,

a source electrode located on one side of said gate electrode, and

a drain electrode located on the other side of said gate electrode.

42. A layered structure for forming electrical devices thereon comprising:

a single crystalline substrate,

a first layer of relaxed $Si_{1-x}Ge_x$ formed epitaxially on said substrate where Ge fraction x is in the range from 0.35 to 0.5,

an over-shoot layer, $Si_{1-y}Ge_y$, within the relaxed structure of said first layer having a Ge fraction y, where $y = x + z$ and z is in the range from 0.01 to 0.1, and having a thickness less than its critical thickness with respect to the top of said first layer, and

a second layer of $Si_{1-x}Ge_x$ formed epitaxially on said first layer.

43. A method for forming p-channel field effect transistors comprising the steps of:

selecting a single crystalline substrate,

forming a first layer of relaxed $Si_{1-x}Ge_x$ formed epitaxially on said substrate where Ge fraction x is

in the range from 0.35 to 0.5,

forming a second layer of $Si_{1-x}Ge_x$ epitaxially on said first layer,

forming a third layer of undoped Si f epitaxially on said second layer,

forming a fourth layer of undoped $Si_{1-x}Ge_x$ f epitaxially on said third layer,

forming a fifth layer of Ge epitaxially on said fourth layer whereby said fifth layer is under compressive strain and has a thickness less than its critical thickness with respect to said first layer,

forming a sixth layer of $Si_{1-w}Ge_w$ epitaxially on said fifth layer where the Ge fraction w is in the range from 0.5 to <1.0 and where $w-x > 0.2$ whereby said sixth layer is under compressive strain, and

forming a seventh layer of $Si_{1-x}Ge_x$ epitaxially on said sixth layer.

44. The method of claim **43** further including the steps of forming an over-shoot layer, $Si_{1-y}Ge_y$, within the strain relief structure of said first layer having a Ge fraction y, where $y = x + z$ and z is in the range from 0.01 to 0.1, and having a thickness less than its critical thickness with respect to said first layer.

45. The method of claim **43** wherein said fifth layer is formed at temperatures where 3D growth of Ge films does not occur to generate interface roughness problems and at a temperature range from 275° - 350° C where 2D growth of Ge films does occur.

46. The method of claim **43** wherein said step of forming a sixth layer includes the step of grading the Ge content *w* within said sixth layer starting with a higher Ge content nearer said fifth layer and grading down in Ge content towards the upper surface of said sixth layer.

47. The layered structure of claim **43** wherein said second layer is a p-doped $Si_{1-x}Ge_x$ layer formed below a channel region of said fifth and sixth layers and separated therefrom by said third layer of Si and said fourth layer of $Si_{1-x}Ge_x$, said second layer is to having a thickness in the range from 1 to 20 nm with a preferred thickness from 4 to 5 nm and having an electrically active donor dose in the range from 1 to $3x10^{12}$ cm^{-2}.

48. A method for forming p-channel field effect transistors comprising:

selecting a single crystalline substrate,

forming a first layer of relaxed $Si_{1-x}Ge_x$ epitaxially on said substrate where Ge fraction *x* is in the range from 0.35 to 0.5,

forming a second layer of $Si_{1-x}Ge_x$ f epitaxially on said first layer,

forming a third layer of undoped Si f epitaxially on said second layer,

forming a fourth layer of Ge epitaxially on said third layer whereby said fourth layer is under compressive strain and having a thickness less than its critical thickness with respect to said first layer,

forming a fifth layer of $Si_{1w}Ge_w$ epitaxially on said fourth layer wherein the Ge fraction w is in the range from 0.5 to <1.0 and where $w\text{-}x > 0.2$ whereby said fifth layer is under compressive strain, and

forming a sixth layer of $Si_{1-x}Ge_x$ epitaxially on said fifth layer.

49. The method of claim **48** further including the step of forming an over-shoot layer, $Si_{1-y}Ge_y$, within the strain relief structure of said first layer having a Ge fraction y, where $y = x + z$ and z is in the range from 0.01 to 0.1, and having a thickness less than its critical thickness with respect to said first layer.

50. The layered structure of claim **48** wherein said fourth layer is formed at temperatures where 3D growth of Ge films does not occur to generate interface roughness problems and at a temperature range from 275° - 350° C where 2D growth of Ge films does occur.

51. The layered structure of claim **48** wherein said step of forming a sixth layer includes the step of grading the Ge content w may be graded within said fifth layer starting with a higher Ge content nearer said fourth layer and grading down in Ge content towards the upper surface of said fifth layer.

52. The method of claim **48** wherein said third layer Si may be substituted with a relaxed $Si_{1-x}Ge_x$ layer with an adjustable thickness to allow the spacer thickness to be varied accordingly whereby the supply dose may be optimized for device applications as a function of temperature in the range from 0.4 to 425K..

53. The method of claim 48 wherein said second layer of p-doped $Si_{1-x}Ge_x$ layer is formed below a channel region of said fourth and fifth layers and separated therefrom by said third layer of Si.

54. The method of claim **52** wherein the supply layer of said second layer is formed and separated below the channel region of said fourth and fifth layers by said relaxed $Si_{1-x}Ge_x$ layer.

55. A method for forming p-channel field effect transistors comprising:

selecting a single crystalline substrate,

forming a first layer of relaxed $Si_{1-x}Ge_x$ epitaxially on said substrate where Ge fraction x is the range from 0.35 to 0.5,

forming a second layer of Ge epitaxially on said first layer whereby said second layer is under compressive strain and having a thickness less than its critical thickness with respect to said first layer,

forming a third layer of $Si_{1-w}Ge_w$ f epitaxially on said second layer where the Ge fraction w is in the range from 0.5 to <1.0 and where w-x > 0.2 whereby said third layer is under compressive strain,

forming a fourth layer of undoped $Si_{1-x}Ge_x$ epitaxially on said third layer,

forming a fifth layer of undoped Si epitaxially on said fourth layer, and

forming a sixth layer of p-doped $Si_{1-x}Ge_x$ epitaxially on said fifth layer.

56. The method of claim **55** further including an over-shoot layer, $Si_{1-y}Ge_y$, within the strain relief structure of said first layer having a Ge fraction y, where $y = x + z$ and z is in the range from 0.01 to 0.1, and having a thickness less than its critical thickness with respect to said first layer.

22. The layered structure of claim **19** wherein said second layer is formed at temperatures where 3D growth of Ge films does not occur to generate interface roughness problems and at a temperature range from 275° - 350° C where 2D growth of Ge films does occur.

57. The method of claim **55** wherein said second layer is formed at temperatures where 3D growth of Ge films does not occur to generate interface roughness problems and at a temperature range from 275° - 350° C where 2D growth of Ge films does occur.

58. The layered structure of claim **55** wherein said step of forming a third layer includes the step of grading the Ge content w within said third layer starting with a higher content nearer said second layer and grading down in Ge content towards the upper surface of said third layer.

59. The method of claim 55 wherein the supply layer of p-doped $Si_{1-x}Ge_x$ layer of said sixth layer is formed above a channel region of said second and third layers and is separated by a composite spacer structure of said fifth layer of Si and said fourth layer of $Si_{1-x}Ge_x$.

60. A method for forming p-channel field effect transistors comprising:

selecting a single crystalline substrate,

forming a first layer of relaxed $Si_{1-x}Ge_x$ epitaxially on said substrate where Ge fraction x is the range from 0.35 to 0.5,

forming a second layer of Ge epitaxially on said first layer whereby said second layer is under compressive strain and has a thickness less than its critical thickness with respect to said first layer,

forming a third layer of $Si_{1-w}Ge_w$ f epitaxially on said second layer where the Ge fraction w is in the range from 0.5 to <1.0 and where $w-x > 0.2$ whereby said third layer is under compressive strain,

forming a fourth layer of undoped $Si_{1-x}Ge_x$ epitaxially on said third layer, and

a fifth layer of p-doped $Si_{1-x}Ge_x$ formed epitaxially on said fourth layer.

61. The method of claim **60** further including the step of forming an over-shoot layer, $Si_{1-y}Ge_y$, within the strain relief structure of said first layer having a Ge fraction y, where $y = x + z$ and z is in the range from 0.01 to 0.1, and having a thickness less than its critical thickness with respect to said first layer.

62. The method of claim **60** wherein said second layer is formed at temperatures where 3D growth of Ge films does not occur to generate interface roughness problems and at a temperature range from 275° - 350° C where 2D growth of Ge films does occur.

63. The method of claim **60** wherein said step of forming a third layer includes the step of grading the Ge content *w* within said third layer starting with a higher content nearer said second layer and grading down in Ge content towards the upper surface of said third layer.

64. The method of claim **60** wherein said fifth layer is a p-doped $Si_{1-x}Ge_x$ layer formed above a channel region of said second and third layers and separated therefrom by said fourth layer of $Si_{1-x}Ge_x$.

65. The layered structure of claim **60** wherein said fifth layer is a p-doped $Si_{1-x}Ge_x$ layer formed above a channel region of said second and third layers and separated therefrom by a thin strained commensurate Si layer.

66. A method of forming a field-effect transistor structure consisting of the method of claim 43, further comprising the steps of,

forming electrical isolation regions by the selective removal of at least said seventh through second layer,

forming a Schottky gate electrode on said seventh layer,

forming a source electrode located on one side of said gate electrode, and

forming a drain electrode located on the other side of said gate electrode.

67. A method for forming a field-effect transistor structure consisting of the method of claim 48, further comprising the steps of,

forming electrical isolation regions by the selective removal of at least said sixth through second layer,

forming a Schottky gate electrode on said sixth layer,

forming a source electrode located on one side of said gate electrode, and

forming a drain electrode located on the other side of said gate electrode.

68. A method of forming a field-effect transistor structure consisting of the method of claim 1, further comprising,

forming electrical isolation regions by the selective removal of at least said seventh through second layer,

forming a gate dielectric on said seventh layer,

forming a gate electrode on said gate dielectric,

forming a source electrode located on one side of said gate electrode, and

forming drain electrode located on the other side of said gate electrode.

69. A method of forming a field-effect transistor structure consisting of the method of claim 48, further comprising the steps of,

forming electrical isolation regions by the selective removal of at least said sixth through second layer,

forming a gate dielectric f on said sixth layer,

forming a gate electrode on said gate dielectric,

forming a source electrode located on one side of said gate electrode, and

forming drain electrode located on the other side of said gate electrode.

70. A method for forming a field-effect transistor structure consisting of the method of claim 55, further comprising,

forming electrical isolation regions by the selective removal of at least said sixth through second layer,

forming a gate dielectric on said sixth layer,

forming a gate electrode on said gate dielectric,

forming a source electrode located on one side of said gate electrode, and

forming a drain electrode located on the other side of said gate electrode.

71. A method of forming a field-effect transistor structure consisting of the method of claim 60, further comprising,

forming electrical isolation regions by the selective removal of at least said fifth through second layer,

forming a gate dielectric formed on said fifth layer,

forming a gate electrode on said gate dielectric,

forming a source electrode located on one side of said gate electrode, and

forming a drain electrode located on the other side of said gate electrode.

72. A method for forming electrical devices comprising the steps of:

forming a single crystalline substrate,

forming a first layer of relaxed $Si_{1-x}Ge_x$ formed epitaxially on said substrate where Ge fraction x is

in the range from 0.35 to 0.5,

forming an over-shoot layer, $Si_{1-y}Ge_y$, within the relaxed structure of said first layer having a Ge fraction y, where $y = x + z$ and z is in the range from 0.01 to 0.1, and having a thickness less than its critical thickness with respect to the top of said first layer, and

forming a second layer of $Si_{1-x}Ge_x$ formed epitaxially on said first layer.